CLAIMS:

1. A semiconductor processing method of forming a conductive transistor gate over a substrate comprising the steps of:

forming a conductive gate over a gate dielectric layer on a substrate, the gate having sidewalls and an interface with the gate dielectric layer;

forming nitride containing spacers over the gate sidewalls; and

after forming the spacers, exposing the substrate to oxidizing conditions effective to oxidize at least a portion of the gate interface with the gate dielectric layer.

2. The semiconductor processing method of claim 1, wherein the gate comprises a first conductive layer a portion of which defines the interface, an overlying metal, and an electrically conductive reaction barrier layer interposed between the first layer and the overlying metal.

3. The semiconductor processing method of claim 1, wherein the gate comprises polysilicon, an overlying metal, and an electrically conductive reaction barrier layer intermediate the polysilicon and the overlying metal.

4. The semiconductor processing method of claim 1, wherein the step of forming the nitride containing spacers includes:

depositing a first nitride containing material over the gate;

depositing a second nitride containing material over the first nitride containing material; and

anisotropically etching the first and second nitride containing materials to a degree sufficient to leave the spacers over the gate sidewalls.

5. The semiconductor processing method of claim 1, wherein the step of forming the nitride containing spacers includes:

depositing a first nitride containing material over the gate;

anisotropically etching the first nitride containing material to a degree sufficient to leave first nitride containing spacers over the gate sidewalls;

depositing a second nitride containing material over the first nitride containing spacers; and

anisotropically etching the second nitride containing material to a degree sufficient to leave second nitride containing spacers proximate the first nitride containing spacers.

6. The semiconductor processing method of claim 1, wherein the step of forming the nitride containing spacers includes:

depositing a first nitride containing material over the gate;

anisotropically etching the first nitride containing material to a degree sufficient to leave first nitride containing spacers over the gate sidewalls;

depositing a second nitride containing material over the first nitride containing spacers; and

anisotropically etching the second nitride containing material to a degree sufficient to leave second nitride containing spacers proximate the first nitride containing spacers, the step of exposing the substrate to oxidizing conditions taking place prior to depositing the second nitride containing material and after anisotropically etching the first nitride containing material.

7. The semiconductor processing method of claim 1, wherein the oxidizing conditions include an ambient temperature in the range from between about 800°C to 1050°C.

8. The semiconductor processing method of claim 1, wherein the gate includes a gate top and further comprising forming an oxidation resistant material over the gate top which, together with the nitride containing spacers, effectively encapsulates the gate.

9. The semiconductor processing method of claim 1, wherein the gate includes a gate top and further comprising forming an nitride containing oxidation resistant material over the gate top which, together with the nitride containing spacers, effectively encapsulates the gate.

10. A semiconductor processing method of forming a conductive gate comprising conducting a gate oxidation step after encapsulating the gate with oxidation resistant material.

11. The semiconductor processing method of claim 10, wherein the step of encapsulating the gate comprises forming electrically insulative sidewall spacers over the gate by:

depositing a first insulative material over the gate;

depositing a second insulative material over the first insulative material; and

anisotropically etching the first and second insulative materials to a degree sufficient to leave the insulative spacers over the gate.

12. The semiconductor processing method of claim 10, wherein the step of encapsulating the gate comprises forming electrically insulative sidewall spacers over the gate by:

depositing a first insulative material over the gate;

anisotropically etching the first insulative material to a degree sufficient to leave first insulative spacers over the gate;

depositing a second insulative material over the first insulative spacers; and

anisotropically etching the second insulative material to a degree sufficient to leave second insulative spacers over the first insulative spacers.

13. The semiconductor processing method of claim 10, wherein the gate comprises polysilicon, an overlying metal, and an electrically conductive reaction barrier layer intermediate the polysilicon and the overlying metal.

14. The semiconductor processing method of claim 10, wherein the oxidation resistant material contains a nitride material.

15. The semiconductor processing method of claim 10, wherein the gate has a gate top and the encapsulating step comprises forming a nitride containing oxidation resistant material over the gate sidewalls and gate top.

16. A semiconductor processing method of forming a conductive transistor gate over a substrate comprising the steps of:

forming a conductive gate over a gate dielectric layer on a substrate, the gate having sidewalls;

forming non-oxide spacers over the sidewalls; and

after forming the spacers, exposing the substrate to oxidizing conditions effective to oxidize at least a portion of the gate and a portion of the substrate beneath the gate.

17. The semiconductor processing method of claim 16, wherein the step of forming the non-oxide spacers comprises:

depositing a first non-oxide material over the gate;

depositing a second non-oxide material over the first non-oxide material; and

anisotropically etching the first and second non-oxide materials to a degree sufficient to leave non-oxide spacers over the gate sidewalls.

18. The semiconductor processing method of claim 16, wherein the step of forming the non-oxide spacers comprises:

depositing a first non-oxide material over the gate;

anisotropically etching the first non-oxide material to a degree sufficient to leave first spacers over the gate sidewalls;

depositing a second non-oxide material over the first spacers; and

anisotropically etching the second non-oxide material to a degree sufficient to leave second spacers over the first spacers.

19. The semiconductor processing method of claim 16, wherein the oxidizing conditions include an ambient temperature from between about 800°C to 1050°C.

20. A semiconductor processing method of forming a conductive transistor gate comprising the steps of:

forming a conductive gate stack over a gate dielectric layer on a substrate; the stack comprising polysilicon, an overlying metal, and an electrically conductive reaction barrier layer intermediate the polysilicon and the overlying metal; the gate having sidewalls and an interface with the gate dielectric layer;

forming an oxidation resistant layer over at least the gate stack sidewalls of the metal; and

after forming the oxidation resistant layer, exposing the substrate to oxidizing conditions effective to oxidize at least a portion of the gate laterally adjacent the oxidation resistant layer.

21. The semiconductor processing method of claim 20, wherein the oxidation resistant layer effectively encapsulates the gate stack.

22. The semiconductor processing method of claim 20, wherein the oxidation resistant layer comprises a nitride material.

23. The semiconductor processing method of claim 20, wherein the oxidation resistant layer comprises an oxidation resistant cap atop the overlying metal, and the step of forming the oxidation resistant layer over at least the gate stack sidewalls of the metal comprises:

depositing a first oxidation resistant layer over the gate;

depositing a second oxidation resistant layer over the first oxidation resistant layer; and

anisotropically etching the first and second layers to a degree sufficient to leave sidewall spacers over at least the gate stack sidewalls between the cap and the dielectric layer.

24. The semiconductor processing method of claim 20, wherein the oxidation resistant layer further comprises an oxidation resistant cap atop the overlying metal, and the step of forming the oxidation resistant layer over at least the gate stack sidewalls of the metal comprises:

depositing a first oxidation resistant layer over the gate;

anisotropically etching the first oxidation resistant layer to a degree sufficient to leave first sidewall spacers over at least the gate stack sidewalls between the cap and the dielectric layer;

depositing a second oxidation resistant layer over the first sidewall spacers; and

anisotropically etching the second oxidation resistant layer to a degree sufficient to leave second sidewall spacers over at least most of the first sidewall spacers.

25. The semiconductor processing method of claim 20, wherein the oxidation resistant layer further comprises an oxidation resistant cap atop the overlying metal, and the step of forming the oxidation resistant layer over at least the gate stack sidewalls of the metal comprises:

depositing a first oxidation resistant layer over the gate;

anisotropically etching the first oxidation resistant layer to a degree sufficient to leave first sidewall spacers over at least the gate stack sidewalls between the cap and the dielectric layer;

depositing a second oxidation resistant layer over the first oxidation resistant layer; and

anisotropically etching the second oxidation resistant layer to a degree sufficient to leave second sidewall spacers over at least most of the first sidewall spacers, the step of exposing the substrate to oxidizing conditions taking place after anisotropically etching the first oxidation resistant layer.

26. The semiconductor processing method of claim 20, wherein the oxidizing conditions include an ambient temperature condition from between about 800°C to 1050°C.

27. A semiconductor processing method of forming a conductive gate comprising:

forming a gate over a gate dielectric layer on a substrate, the gate having sidewalls;

shielding at least a portion of the gate sidewalls with a nitride containing oxidation resistant material; and

after the shielding, exposing the substrate to oxidation conditions effective to oxidize at least a portion of the gate sidewalls laterally inwardly of the oxidation resistant material, the shielding channeling oxidants through the gate dielectric layer to the gate sidewalls.

28. The semiconductor processing method of claim 27, wherein the shielding step comprises covering a top of the gate with the oxidation resistant material.

29. The semiconductor processing method of claim 27, wherein the shielding step comprises covering the gate with the oxidation resistant material in at least two separate steps.

30. The semiconductor processing method of claim 27, wherein the gate comprises polysilicon, an overlying metal, and an electrically conductive reaction barrier layer intermediate the polysilicon and the overlying metal.

31. The semiconductor processing method of claim 27, wherein the gate comprises polysilicon, an overlying metal, and an electrically conductive reaction barrier layer intermediate the polysilicon and the overlying metal, a portion of the overlying metal defining a gate top, and the shielding step further comprises forming an oxidation resistant cap atop the gate top.

32. The semiconductor processing method of claim 27, wherein the oxidizing conditions include an ambient temperature from between about 800°C to 1050°C.

33. A semiconductor processing method of forming a conductive gate comprising the steps of:

forming a patterned gate atop a substrate dielectric surface, at least a portion of the gate being conductive;

covering a top and sidewalls of the gate with oxidation resistant material; and

exposing the substrate to oxidation conditions effective to oxidize at least a portion of the gate laterally adjacent the covered sidewalls adjacent the dielectric surface.

34. The semiconductor processing method of claim 33, wherein the conductive portion of the gate comprises a reaction barrier layer and an overlying metal thereon.

35. The semiconductor processing method of claim 33, wherein the conductive portion of the gate comprises polysilicon, an overlying metal, and a reaction barrier layer interposed between the polysilicon and the overlying metal.

36. The semiconductor processing method of claim 33, wherein the covering step comprises:

depositing a first barrier material over the gate;

depositing a second barrier material over the first barrier material; and

anisotropically etching the first and second barrier materials to a degree sufficient to leave the oxidation barriers on the gate.

37. The semiconductor processing method of claim 33, wherein the covering step comprises:

depositing a first barrier material over the gate;

depositing a second barrier material over the first barrier material; and

anisotropically etching the first and second barrier materials to a degree sufficient to leave the oxidation barriers on the gate, the etched first barrier material defining at least one L-shaped oxidation barrier.

38. The semiconductor processing method of claim 33, wherein the covering step comprises:

depositing a first barrier material over the gate;

anisotropically etching the first barrier material to a degree sufficient to leave first oxidation barriers on the gate;

depositing a second barrier material over the first barrier material; and

anisotropically etching the second barrier material to a degree sufficient to leave second oxidation barriers over the first oxidation barriers.

39. The semiconductor processing method of claim 33, wherein the oxidation resistant material comprises a nitride material.

40. A semiconductor processing method of forming a conductive line comprising:

forming a conductive line atop a substrate dielectric layer;

covering a top and sidewalls of the conductive line with at least one nitride material; and

oxidizing a portion of the conductive line laterally inwardly of the nitride material.